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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/740,455	12/18/2000	Susie Go	10003527-1	4919

7590 07/02/2004

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
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EXAMINER	
PALADINI, ALBERT WILLIAM	

ART UNIT	PAPER NUMBER
2125	

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/740,455	GO ET AL.	
	Examiner	Art Unit	
	Albert W Paladini	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 1-15 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements and structural cooperative relationships of elements, such omission amounting to a gap between the necessary elements and structural connections. See MPEP § 2172.01.

Claim 1

The preamble recites an apparatus. An apparatus claim must contain all of the physical elements and the interconnections between all of the elements necessary to perform the desired function.

The claim recites "logic' and treats it as if it were a physical element. Then the claim continues to list a multitude of functions that the undefined apparatus "logic" performs.

Lines 3-4 recite, "wherein when the first logic performs the system design algorithm." There is no antecedent basis for "first logic." Here again, "logic" is not a physical element. There is not recitation of the elements to perform the "system design algorithm."

To be a complete apparatus claim, it must recite all of the elements and the structural or functional connections between the elements. For a structural claim, the

recitation must describe clearly how all the elements are physically connected together. For a functional claim, the recitation must describe clearly how the elements are physically connected together, and in addition, the sequential logical operation of the element working cooperatively together must be understood. For a method claim, the recitation must describe a sequential operation where each step further limits the previous step. In addition, even though the method claim is procedural, each step must be supported with sufficient physical means for accomplishing the step.

This claim appears to attempt to provide a framework for a set of operations under the guise of an apparatus claim. However, it is not complete as an apparatus claim for the reasons given above. The claim is written in narrative form suggesting a number of functions, which might be performed such as clustering and calculating. It is not a complete or comprehensive apparatus claim, and it is not a method claim.

Claim 2

The preamble recites an apparatus. An apparatus claim must contain all of the physical elements and the interconnections between all of the elements necessary to perform the desired function.

The claim recites "logic' and treats it as if it were a physical element. Then the claim continues to list a multitude of functions that the undefined apparatus "logic" performs.

Lines 2-3 recite, "wherein when the first logic performs the storage system design algorithm." There is no antecedent basis for "first logic." Here again, "logic" is not

a physical element. There is not recitation of the elements and their interconnections, which perform this "storage system design algorithm."

To be a complete apparatus claim, it must recite all of the elements and the structural or functional connections between the elements. For a structural claim, the recitation must describe clearly how all the elements are physically connected together. For a functional claim, the recitation must describe clearly how the elements are physically connected together, and in addition, the sequential logical operation of the element working cooperatively together must be understood. For a method claim, the recitation must describe a sequential operation where each step further limits the previous step. In addition, even though the method claim is procedural, each step must be supported with sufficient physical means for accomplishing the step.

This claim appears to attempt to provide a framework for a set of operations under the guise of an apparatus claim. However, it is not complete as an apparatus claim for the reasons given above. The claim is written in narrative form suggesting a number of functions, which might be performed such as clustering and calculating. It is not a complete or comprehensive apparatus claim, and it is not a method claim.

Claim 22

Lines 3-4 recite "a first code segment for clustering stores to produce a cluster workload that reduces a number of constraint calculations that need to be performed per store." The recitation states an objective or advantage of reducing "a number of constraint calculations," but provides no means for accomplishing this. The optimization

scheme suggested in the recitation appears to be the key element that is possibly unique. But a mere statement that an element of an invention performs a function such as an optimization technique is not sufficient support.

Appropriate correction and clarification are required.

3. Claims 16-21 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

Claim 16

The first step recited in the claim is "ordering stores to be clustered." The steps are missing which set the criteria for selecting the stores to be clustered. It is assumed that this method is performed by a processor or computing device. Even if it were a random selection, some criteria would be set for ordering such as *randomly select k out of n stores to be clustered.*

The second step recites, "clustering the stores." This suggests dividing the stores ordered into smaller groups or clusters. There are no steps, which recite the criteria for grouping subsets of stores together.

Step three recites "assigning the cluster workload," The step or steps, which recite the basis, criteria, and methodology of assigning the cluster workload, are missing. These do not appear to be tasks assigned to an individual who makes arbitrary decisions for each step.

Although the specification provides a dictionary for the claims, and the claims may be broader than the specification; each claim must be complete and self consistent in itself. For a structural claim, the recitation must describe clearly how all the elements are physically connected together. For a functional claim, the recitation must describe clearly how the elements are physically connected together, and in addition, the sequential logical operation of the element working cooperatively together must be understood. For a method claim, the recitation must describe a sequential operation where each step further limits the previous step. In addition, even though the method claim is procedural, each step must be supported with sufficient physical means for accomplishing the step.

Appropriate correction and clarification are required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wuytack (6421809).

This rejection is made to the extent that the claims are understood by addressing elements and or steps recited as related to the objective of the invention.

Wuytack discloses a system and apparatus for designing constraint based storage systems. He teaches optimization techniques utilized in storage clustering on lines 62 column 1 to line 11 column 2 where he states "In the parallel compiler domain [M. Al-Mouhamed, S. Seiden, A Heuristic Storage for Minimizing Access Time of Arbitrary Data Paterns, IEEE Transactions on Parallel and Distributed Systems, Vol.8, No.4, pp.441-447, Apr. 1997.] proposes a technique to partition arrays into groups of data that have to be assigned to different memories such that they can be accessed simultaneously for an SIMD architecture. They combine the constraints of a number of given access patterns into a single linear address transformation that calculates for every data element the memory in which it should be stored to minimize the total access time. This technique allows to avoid the allocation of multi-port memories for storing data with self-conflicts, by explicitly splitting arrays into smaller arrays that can be assigned to single port memories. However said method does not exploit all optimization opportunities for instance by rescheduling data access instructions." Wuytack does not explicitly state that the technique minimizes the number of constraint calculations.

However, since Wuytack does combine the constraints of a number of access patterns into a single linear address to minimize total access time, it would have been obvious to one of ordinary skill in the art that the number of constraint calculations is also minimized.

Relevant Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chen (5475830) discloses a method and structure for implementing circuit designs, which includes a clock analysis module identifying clock paths, a clustering module

which clusters each storage instance with (i) the data paths leading to a data input terminal of the storage instance and (ii) the local clock path of the clock signal to the storage instance. A partition module assigns the components of each cluster is implemented by the same programmable logic device so as to minimize delay in the data path In that embodiment, "different clock" storage instances are assigned different clocked programmable logic devices ("clocked FPGAs"), and the delay of the delay constraint is provided by an unclocked programmable logic device ("unclocked FPGA"). Further, a connectivity module provides a connectivity graph indicating connectivity between clusters. Additionally, a data structure associated with a component common to multiple clusters notes the clusters in which the component is present. When a pair of clusters having duplication are implemented in separate programmable devices, the common circuits are duplicated in each programmable device to minimize the need for interchip interconnections, and preserve circuit performance.

Balasa (5742814) discloses a memory allocation system and method which includes a background memory allocation which is modeled as a global optimization problem, which minimizes the estimated storage area in silicon, while complying with imposed performance and partial ordering constraints. The data-flow driven allocation can be extended in order to deal with more complex cost functions based on area and power models for on-chip memories. The result of the background memory allocation consists of a distributed (multiport) memory architecture with fully-determined characteristics, having a minimal total area, and complying with a given clock cycle budget for read/write operations.

Dangelo (6324678) discloses a mythology for generating structural descriptions of digital devices including a process which iterates through checking whether the constraints

are met, calculates a "cost function" based on the prioritization of the constraints, then seeks to minimize the cost function by moving functional units from one partition to another, or by adding redundant units to one or more partitions.

8. Any inquiry concerning this communication or earlier communication from the examiner should be direct to Albert W. Paladini whose telephone number is (703) 308-2005. The examiner can normally be reached from 7:30 to 3:30 PM on Monday, Tuesday, Thursday, and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Leo P. Picard, can be reached on (703) 308-0538. The official fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Albert W. Paladini
Primary Examiner
Art Unit 2125

June 28, 2004